I claim:

1. A vertical non-volatile semiconductor memory cell, comprising:

a substrate having a surface, a drain region, a channel region and a source region;

a trench that is formed in said substrate from said source region to said drain region, said trench formed vertically, essentially perpendicular to said surface of said substrate, said trench having trench walls;

a first dielectric layer that is formed essentially on said trench walls;

a charge storage layer for storing charges, said charge storage layer having a surface and essentially being formed on said first dielectric layer;

a second dielectric layer that is formed at least partially on said surface of said charge storage layer;

a control layer that is formed essentially on said surface of the second dielectric layer and that has a surface;

a trench extension that is formed essentially underneath said trench, said trench extension having a surface;

a third dielectric layer located on said surface of said trench; and

a filler material for at least partially filling said trench extension.

2. The vertical non-volatile semiconductor memory cell according to patent claim 1, wherein said filler material electrically isolated from said charge storage layer.

3. The vertical non-volatile semiconductor memory cell according to patent claim 1, wherein said filler material is in electrical contact with said charge storage layer.

4. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer and said control layer extend at least partially within said trench.

5. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer and said control layer extend at least partially within said trench and said trench extension.

6. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer and said control layer extend at least partially within said trench, said trench extension and said substrate.

7. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said first dielectric layer has a tunnel layer.

8. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer includes an ONO layer sequence and said third dielectric layer includes an ONO layer sequence.

9. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said second dielectric layer has a dielectric with a high relative dielectric constant.

10. The vertical non-volatile semiconductor memory cell according to claim 9, wherein said second dielectric layer has a metal oxide.

11. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said filler material, said charge storage layer and said control layer include a material

selected from the group consisting of an electrically conductive polysilicon and a silicide.

12. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said control layer includes a surface layer and at least one control filler layer.

13. The vertical non-volatile semiconductor memory cell according to claim 1, wherein said trench and said trench extension constitute a deep trench that is formed in a DRAM process.

14. A method for manufacturing a vertical non-volatile semiconductor memory cell, which comprises:

providing a substrate;

forming a deep trench in the substrate, providing the deep trench with a third dielectric layer, and filling the deep trench with a filler material;

partially removing the filler material and the third dielectric layer in the deep trench to form an upper trench;

forming a first dielectric layer in the upper trench;

forming a charge storage layer in the upper trench;

forming a control layer trench at least partially in the charge storage layer;

forming a second dielectric layer in the control layer trench;

forming a control layer in the control layer trench; and

forming a collar isolation, a flat trench isolation and connecting elements.

15. The method according to claim 14, which comprises etching the control layer trench into the upper trench.

16. The method according to claim 14, which comprises etching the control layer trench into the deep trench.

17. The method according to patent claim 14, which comprises etching the control layer trench into the substrate.